

# Power Site™

Automated Power  
Semiconductor Attachment

*Cool.*

*Reliable.*

*Hardware-free.*

**Direct solder mounting of power semiconductors to heat sinks...**

# Power Site™ **without mechanical fasteners**

Automated Power Semiconductor Attachment  
Patented

## Introducing “SIMS” – Selectively Insulated Metal Substrate

Chomerics' fully automated PowerSite technology provides precise, **selective** positioning of electrically isolated copper interface pads **only** where power devices are to be soldered onto heat sinks. Material cost for the device attachment is minimized, and automation lowers labor expense and ensures consistency.

*This new technology offers important performance benefits:*

### Hardware-free mounting reduces parts count, saves space

PowerSite technology saves valuable package space, because power semiconductor devices are soldered directly to the copper patches, with no fasteners required. There are no screws, nuts, rivets, clips or brackets to inventory, no fastener holes to compromise thermal or electrical integrity.

Pressure dependency associated with mounting hardware is no longer an issue. Neither is the problem of fasteners becoming loose over time. The high repeatability of automated processing replaces the variability of manual hardware installation.

### Improved thermal performance

With thermal impedance as low as  $0.1^{\circ}\text{C}\text{-in}^2/\text{W}$  ( $0.65^{\circ}\text{C}\text{-cm}^2/\text{W}$ ), PowerSite patches deliver 2 to 5 times that achieved with conventional, manually-applied thermal interface pads. This improved performance offers the designer an opportunity to:

- lower device temperature
- reduce heat sink size
- elevate power capacity
- increase ambient temperature rating

### Advanced all-polyimide construction provides a strong, durable bond

The PowerSite assembly process is a high temperature lamination of 1-oz. copper foil to the aluminum heat sink substrate. This is accomplished with a proprietary, chemical-resistant insulation utilizing Kapton\* MT polyimide film that has been coated with polyimide adhesive on each side. Precise positioning of the insulation film and copper foil, followed by lamination under elevated pressure and heat, is fully automated in one piece of process equipment. The finished patches are ready for immediate device soldering, which can be integrated as the final step.

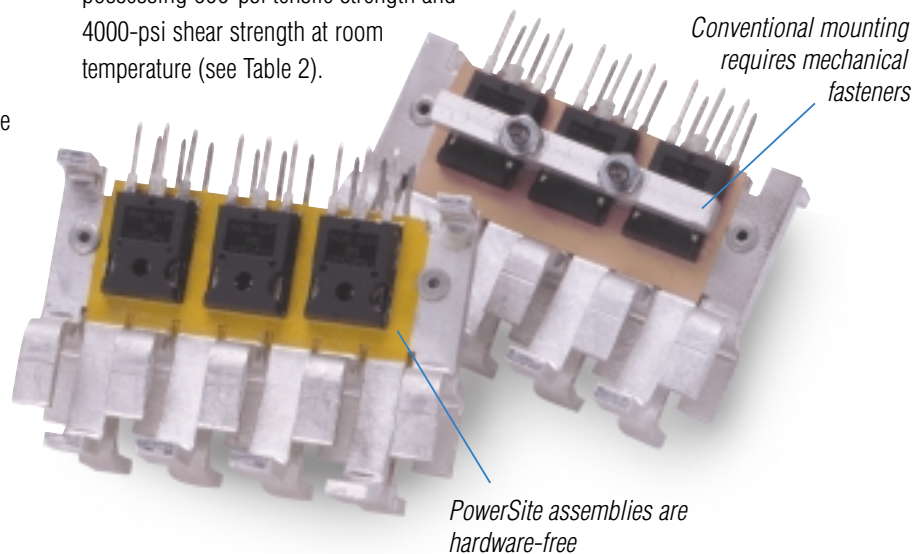
The PowerSite process produces bonds possessing 600-psi tensile strength and 4000-psi shear strength at room temperature (see Table 2).

### Dielectric reliability

Reliable electrical insulation is ensured with the durable Kapton\* MT film layer and polyimide adhesive, achieving a voltage breakdown of 5000 Vac (see Table 2).

### Finned or contoured heat sinks

PowerSite process equipment can accommodate virtually any heat sink design, including those with elaborate fin structures. This is a major departure from the flat panel requirement of existing insulated metal substrate (IMS<sup>+</sup>) processing.



## Bonded parts or complete subassemblies

Chomerics will bond PowerSite patches to customer-supplied heat sinks, which are then ready for device soldering. If desired, Chomerics will solder power semiconductors to the patches, providing complete subassemblies.

Chomerics can also serve as lead vendor, managing the supply chain for heat sinks and power devices. In addition, Chomerics will license PowerSite processing equipment to volume manufacturers, and supply the specialized PowerSite materials.

## Withstands environmental stress - thermal performance unaffected

Long-term thermal performance of PowerSite patches depends on the reliability and repeatability of the lamination. Environmental stressing designed to test the integrity of the lamination at the aluminum/bond film and copper/bond film interfaces, as well as the solder joint, has been conducted. Thermal resistance of the samples was measured before and after stress using an Analysis Tech Phase VI Thermal Analyzer.

In all cases, the integrity of the lamination was maintained and the solder joint was unaffected. No significant change in thermal resistance was observed after testing under conditions summarized in Table 1. (A copy of the test method and detailed test results are available on request.)

Table 1

ENVIRONMENTAL STRESS TESTING	
Test	Conditions
High Temperature Aging	1000 hrs at 150°C
Thermal Shock, liquid-to-liquid	200 cycles, -50 to +150°C
Thermal Cycling	1000 cycles, -50 to +150°C
High Heat and Humidity	1000 hrs at 85°C/85% RH

Table 2

TYPICAL PROPERTIES			
Property		PowerSite Laminate	Test Method
CONSTRUCTION	Copper Thickness, inch (mm)	0.0014 (0.036)	ASTM D374
	Thermoplastic Polyimide (TPI) Adhesive Thickness, inch (mm)	0.00015 (0.004)	ASTM D374
	Kapton MT Dielectric Thickness, inch (mm)	0.001 (0.025)	ASTM D374
	Thermoplastic Polyimide (TPI) Adhesive Thickness, inch (mm)	0.00015 (0.004)	ASTM D374
THERMAL	Laminate Thermal Impedance, °C-in <sup>2</sup> /W (°C-cm <sup>2</sup> /W)	0.1 (0.65)	ASTM D5470-95
	Dielectric Thermal Conductivity, W/m-k	0.38	ASTM D5470-95
	Operating Temperature Range, °C	-50 to +200	—
	Junction-to-Heat Sink Thermal Resistance, R <sub>j-s</sub> , °C/W* TO-247 TO-220	0.67 2.67	JEDEC Std 51 using Analysis Tech Thermal Analyzer
ELECTRICAL	Voltage Breakdown, Vac	5000	ASTM D149
	Volume Resistivity, ohm-cm	1 x 10 <sup>14</sup>	ASTM D257
	Capacitance, pF/in <sup>2</sup> (pF/cm <sup>2</sup> )	500 (78)	ASTM D150
	Permittivity, 25°C @ 1kHz	4	ASTM D150
	Dissipation Factor, 25°C @ 1kHz	0.003	ASTM D150
MECHANICAL	Tensile Strength, psi (mPa) Room Temp 150°C	600 (4.1) 200 (1.4)	ASTM D412
	Shear Strength, psi (mPa) Room Temp 150°C	4000 (27.6) 2000 (13.8)	ASTM D412
	UL Recognized	Pending	—

\*Includes component's internal junction-to-case thermal resistance.

## Which applications benefit most from PowerSite technology?



### POWER SUPPLIES

**Limited space and weight** – Eliminating bulky hardware frees up space and trims package weight.

**Production volumes** – Any operation mounting 50,000 or more power semiconductors per year will benefit from PowerSite process efficiencies.

**High heat loads** – As power levels rise, the advantages of PowerSite attachment increase. TO-220 devices with >3 watts and TO-247 devices with >7 watts of dissipation are well suited for PowerSite attachment.

**Non-flat heat sink profiles** – Finned and contoured heat sinks with non-planar features are no problem for PowerSite assembly equipment. This circumvents the 18x24 inch (46x61 cm) flat panel format of traditional IMS processes, and the secondary process of subdividing panels.



### MOTOR CONTROLS

**Processing** – Assemblies with four or more power devices are excellent candidates for PowerSite attachment.

**Heat sink thermal performance** – The better the heat sink is, the greater the performance advantage gained with PowerSite technology's lower interface resistance.

**Heat sink size** – PowerSite process equipment handles heat sinks weighing as much as 1000 gm or more, with footprints as large as 8x12 inches (20x30 cm).

**Fewer interfaces** – By mounting directly to the heat sink, PowerSite patches eliminate the substrate-to-heat sink interface common in IMS applications.



### AUTOMOTIVE ELECTRONICS

**Table 3**

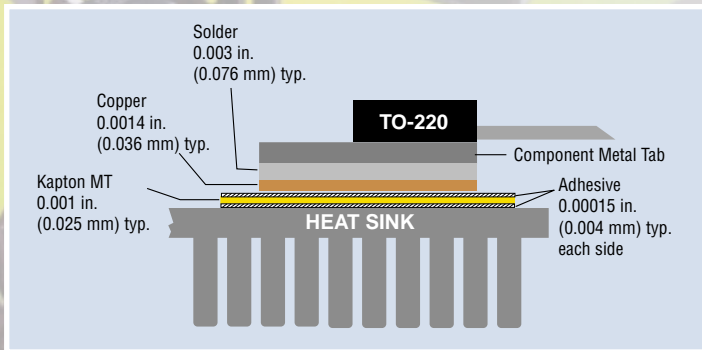
<b>THERMAL INTERFACE TECHNOLOGIES COMPARISON</b>					
<i>Application</i>	<b>Device Mounting</b>			<b>Power Circuitry</b>	<b>Die Mounting</b>
<i>System</i>	<b>MICA/GREASE</b>	<b>INSULATOR PADS</b>	<b>PowerSite™ (SIMS)</b>	<b>INSULATED METAL SUBSTRATE</b>	<b>DIRECT BOND COPPER</b>
<i>Introduced</i>	pre-1940	1960s	2001	1980s	1960s
<i>Insulation Construction</i>	Mica wafer with thermal grease on both sides	Filled silicone binder coated on glass fabric or Kapton film	Polyimide adhesive-coated Kapton MT film	Polymer/ceramic blend	Ceramic wafer
<i>Typical Dielectric Layer Thickness, inch (mm)</i>	0.002 to 0.005 (0.05 to 0.13)	0.005 to 0.020 (0.13 to 0.51)	0.0013 (0.033)	0.006 to 0.012 (0.15 to 0.30)	0.015 to 0.040 (0.38 to 1.00)
<i>Device Attachment</i>	Hardware compression	Hardware compression	Soldering	Soldering	Soldering
<i>Typical Thermal Performance</i>	High 0.1°C-in <sup>2</sup> /W (0.65°C-cm <sup>2</sup> /W)	Low 0.3 to 0.5°C-in <sup>2</sup> /W (1.94 to 3.23°C-cm <sup>2</sup> /W)	High 0.1°C-in <sup>2</sup> /W (0.65°C-cm <sup>2</sup> /W)	High 0.1°C-in <sup>2</sup> /W (0.65°C-cm <sup>2</sup> /W)	Highest 0.05°C-in <sup>2</sup> /W (0.32°C-cm <sup>2</sup> /W)
<i>Advantages</i>	High thermal performance  Low cost	Low cost, clean installation  Design versatility  Easiest rework	Automated Hardware-free  Finned and non-planar heat sinks  Copper applied only at device site  Consistent thermal transfer  Eliminates substrate-to-heat sink interface  Polyimide durability and high dielectric strength	Automated Hardware-free  Simultaneous device pad and circuit pattern etch  Consistent thermal transfer	Very high thermal performance  Automated Hardware-free  Simultaneous device pad and circuit pattern etch  Can accommodate thick copper layer
<i>Potential Disadvantages</i>	Messy, time consuming  Attachment hardware  Inconsistent, uneven coverage  Dry out over time  Contamination of adjacent circuitry	Attachment hardware  Thermal transfer is pressure-dependent  Heat sink modifications (holes, etc.)  High mounting pressure can cause cut-through failures	Assembled with special process equipment  Rework requires solder reflow	Dielectric variability, reliability  Rework requires solder reflow  Large, flat panels only  Brittle - limits design, processing  De-panelizing step required  Can require heat sinks  Copper etch process required	Rework requires solder reflow  High cost  Brittle - limits design, processing  Can require heat sinks  Processed in small panels  Copper etch process required

***Our PowerSite technology specialists are ready to assist you in streamlining your manufacturing process***

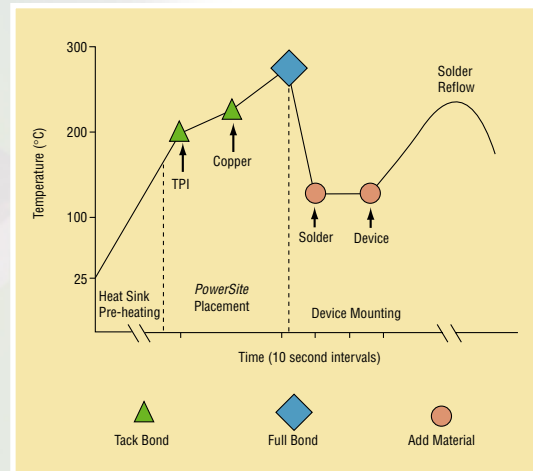


\*Kapton is a trademark of DuPont.  
 †IMS is a trademark of Bergquist Corporation

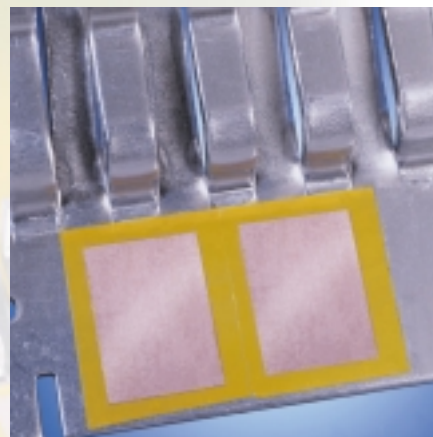
- **“SIMS” – Selectively Insulated Metal Substrate technology**
- **cost-effective, automated process ensures consistency**
- **lower device operating temperatures**
- **use virtually any heat sink design**
- **increase operating power without raising component junction temperature**
- **low thermal variability, no pressure dependency**
- **compatible with all standard solder-mountable packages – TO-220, TO-247, TO-218, etc.**



Typical cross section (not to scale)

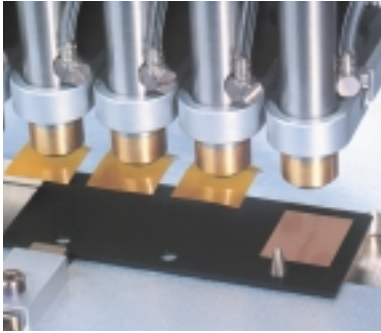


PowerSite process conditions are the same regardless of equipment configuration.

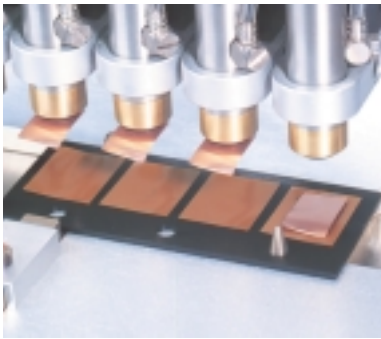


Chomerics' PowerSite process creates a Selectively Insulated Metal Substrate (SIMS), in which electrically isolated copper patches are bonded to a heat sink only where power devices are to be soldered. The patches provide a low thermal impedance interface for direct soldering of power semiconductor packages.

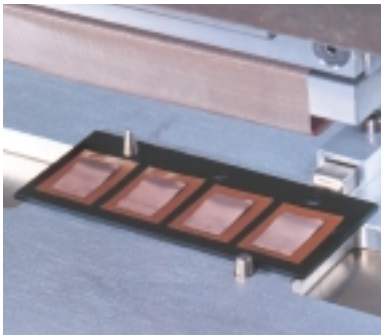
## PowerSite COST-EFFECTIVE AUTOMATED ASSEMBLY



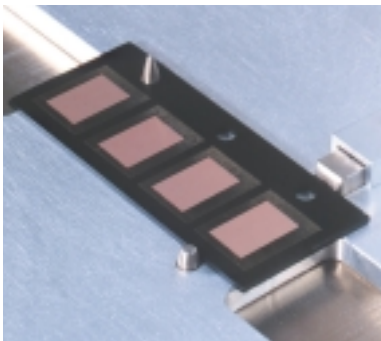
*Pre-cleaned heat sinks are positioned on pre-heating block. Custom-cut Kapton MT pads are then precisely positioned and tack bonded to the substrate.*



*Copper foil is placed and tack bonded.*



*The assembly undergoes 10-second exposure to 600 psi at 300°C.*



*PowerSite patches are immediately ready for direct soldering of power devices. The solder attach process is integrated into the automated PowerSite work cell.*

*Batch scale and continuous production systems are available.*



*Chomerics is a division of the Seal Group of the Parker Hannifin Corporation. Parker Seal is one*

*of the world's largest and most experienced manufacturers of elastomer and other sealing and shielding devices.*

**Chomerics**  
**Div. of Parker Hannifin**  
77 Dragon Court  
Woburn, MA 01888-4014  
TEL: +(1) 781-935-4850  
FAX: +(1) 781-933-4318



**Parker Hannifin PLC**  
**Chomerics Europe**  
Parkway, Globe Park Estate  
Marlow, Bucks., SL7 1YB, England  
TEL: +(44) 1628 404000  
FAX: +(44) 1628 404090



**Parker Hannifin Asia Pacific Group**  
Chomerics Sales Department  
8/F, Kin Yip Plaza  
9 Cheung Yee Street  
Cheung Sha Wan  
Kowloon, Hong Kong  
TEL: +(852) 2428 8008  
FAX: +(852) 2423 8253

**Parker Hannifin Ind. e Com. Ltda.**  
Seals Division  
Via Anhanguera, KM 25,3-Perus  
05276-977-São Paulo-SP, Brazil  
TEL: +(55) 11 3917 1099  
FAX: +(55) 11 3917 0817

[www.chomerics.com](http://www.chomerics.com)

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